Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An integrated circuit incorporating microelectromechanical systems (MEMS), ~~having a total area greater than an area of at least one of the reticles used to manufacture it~~ wherein the integrated circuit comprises a plurality of first reticle exposed areas having logic circuitry, and a plurality of second reticle exposed areas having pads.

2. – 6. (Cancelled)

7. (Withdrawn) A method of manufacturing an integrated circuit incorporating MEMS, comprising laying out the integrated circuit using a plurality of overlapping reticles.

8. (Withdrawn) A method according to claim 7, wherein the overlapping reticles are the same as each other.

9. (Withdrawn) A method according to claim 7, wherein the reticles are different to each other.

10. (Withdrawn) A method according to claim 9, wherein the reticles are different lengths.

11. (Withdrawn) A method of manufacturing an integrated circuit printhead according to claim 7.

12. (Withdrawn) A method of manufacturing a plurality of integrated circuits on a single substrate wafer, wherein each of the integrated circuits is manufactured in accordance with claim 7.

13. (Withdrawn) A method according to claim 12, wherein at least some of the integrated circuits are different to each other.

14. (Withdrawn) A method according to claim 13, wherein the integrated circuits are of different lengths.

15. (Withdrawn) A method laying out an integrated circuit according to claim 1, the method including the steps of:

defing a layout of an integrated circuit;

defining a joint path;

modifying at least one element within an overlap area adjacent the joint path to take into account reticle field overlap during a subsequent manufacturing step.

16. (New) An integrated circuit according to claim 1, wherein each first reticle exposed area includes a first end and a second end, each second reticle exposed area includes a first and second end, and wherein the second end of some of the plurality of first reticle exposed areas border the first end of some of the plurality of second reticle exposed areas.

17. (New) An integrated circuit according to claim 16, wherein the first end of some of the plurality of first reticle exposed areas border the second end of some of the plurality of second reticle exposed areas.

18. (New) An integrated circuit according to claim 1, wherein the integrated circuit is a printhead integrated circuit.

19. (New) An integrated circuit according to claim 18, wherein the logic circuitry comprises an array of nozzle logic circuitry.

20. (New) An integrated circuit according to claim 1, wherein the plurality of first reticle exposed areas seals the integrated circuit.

21. (New) An integrated circuit according to claim 1, wherein the plurality of first reticle exposed areas forms a feedback circuit.

22. (New) An integrated circuit according to claim 1, wherein the integrated circuit includes a plurality of reticle exposed arrays each reticle exposed array comprising a plurality of first reticle exposed areas and a plurality of second reticle exposed areas.

23. (New) An integrated circuit according to claim 22, wherein each reticle exposed array is positionally offset relative to bordering reticle exposed arrays.

24. (New) An integrated circuit according to claim 1, wherein each first reticle exposed area and each second reticle exposed area has a maximum longitudinal length of 23 millimeters.